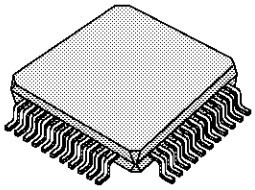
SGS-THOMSON MICROELECTRONICS

STV6407

VIDEO MATRIX

- 6 CVBS INPUTS - 3 CVBS OUTPUTS
- 4 Y/C INPUTS - 2 Y/C OUTPUTS
- 2 EXTRA Y/C INPUTS FOR EXTERNAL COMB FILTERS
- 3 Y/C ADDERS (ONE WITH EXTERNAL TRAP FILTER)
- CLAMP MODE : SYNC BOTTOM ON CVBS AND Y INPUTS, AVERAGE ON C INPUTS
- S SELECTED INPUT FORWARDED TO SOUT PIN (auto mode) OR PROGRAMMABLE (soft mode)
- BANDWIDTH : 15MHz
- CROSSTALK : 50dB min.
- STATUS REGISTER AVAILABLE THROUGH I^2C BUS (S1, S2, S3, ID1-1, ID1-2)
- 2 SELECTABLE SLAVE ADDRESSES
- I^2C BUS CONTROL



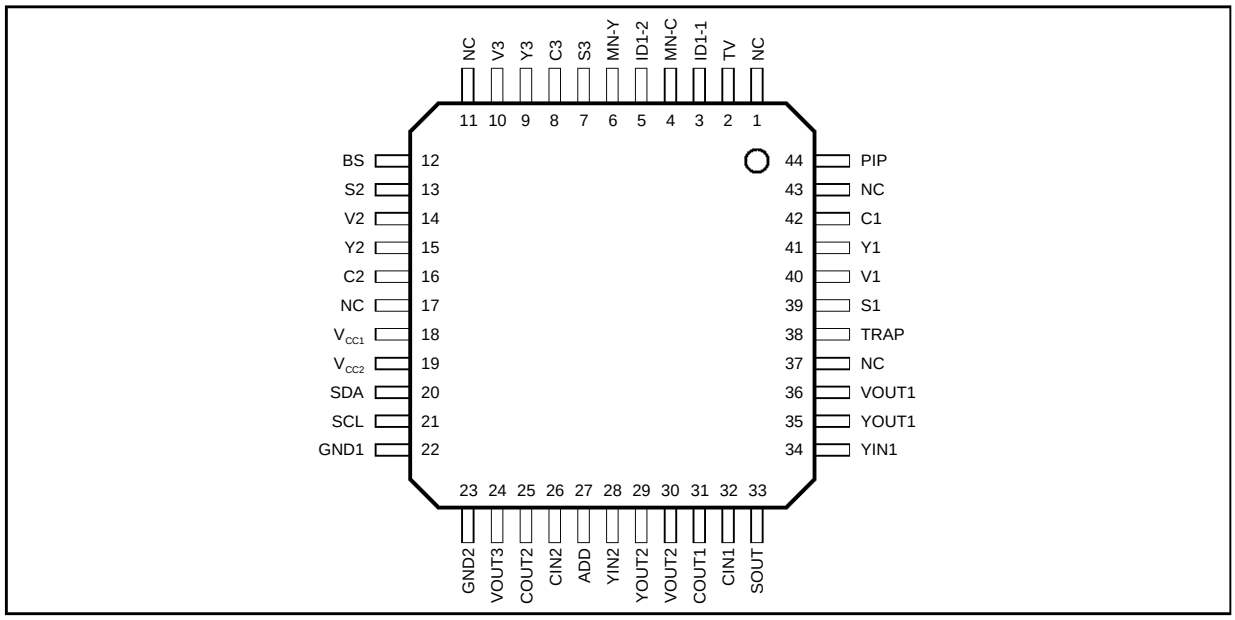
PQFP44
(Plastic Quad Flat Pack)

ORDER CODE : STV6407

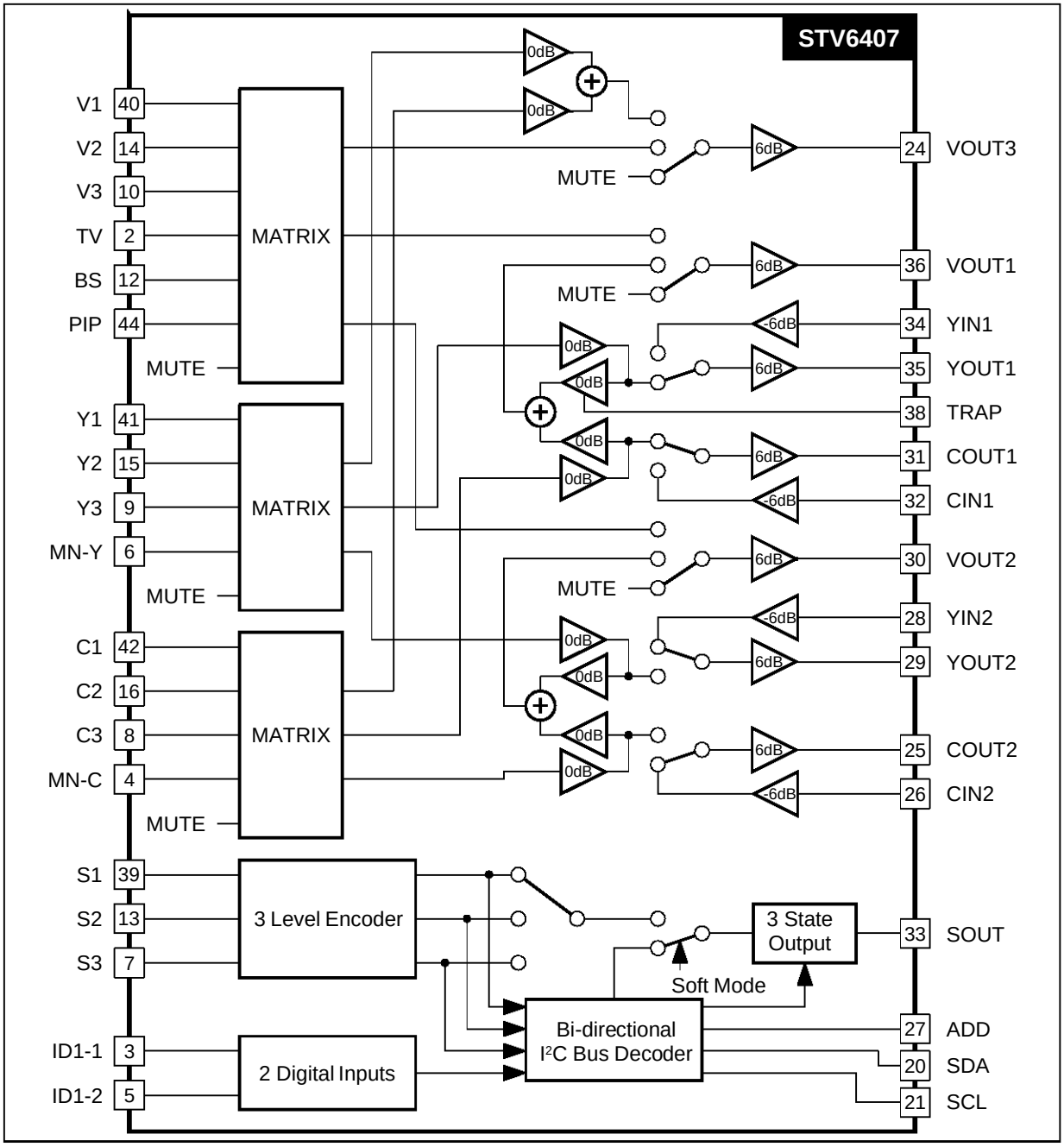
DESCRIPTION

This device is an I^2C bus controlled video switch dedicated to TV applications. It handles video or chroma input signals, filtered or not, which are forwarded to selected outputs.

PIN CONNECTIONS



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The STV6407 is basically composed of 3 sets of CVBS and Y/C inputs which can be commuted through I^2C bus control to respective CVBS or Y/C outputs.

All CVBS and Y input signals are synchro bottom clamped, while C signals are average. Thanks to internal Y/C adders and amplifiers, it is possible to generate additional CVBS signals depending on the selected output group.

Every output VOUT1, VOUT2 and VOUT3 supplies a CVBS signal issued from either a CVBS input or from added Y/C signals. Thanks to an external trap filter connected to the TRAP input, the Y signal from Y matrix can be filtered before being combined to C signal from C matrix and then directed to VOUT1.

YOUT1/COUT1 and YOUT2/COUT2 deliver Y/C signals coming from external comb filters if input is a CVBS source or from Y/C sources if Y/C sources are used.

Besides switching function, the STV6407 outputs a control signal on SOUT pin which can be related to the selected switching group or can be used to drive other devices according to either of the 2 programming modes :

- In the former mode, SOUT supplies the encoded signal received through 3 level encoders from S1, S2 or S3 input when the corresponding switching input group (V1, Y1, C1 or V2, Y2, C2 or V3, Y3, C3) is selected and if b5 of control register is reset. If b5 = 1, SOUT is unchanged when a new input group is selected. For example, if V3, Y3, C3 is selected and then if b5 = 0, SOUT will reflect S3 input level : if S3 input voltage changes, SOUT will be automatically updated.
- In the latter mode, SOUT can be driven directly through I^2C bus. This mode, called SOFT MODE (b7 = b6 = 1, b5 = b4 = b1 = b0 = 0), allows 4 different settings of SOUT : 0V, 2.5V, 5V or high impedance. SOUT can then be used to drive other interface devices or plugs (pin 8 of SCART plugs).

The status register readable through I^2C bus indicates status of the two logical encoders ID1-1 and ID1-2 (bits b0 and b1) and of S1, S2 and S3 inputs (bits b2 to b7).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7	V
V_I	Voltage at Pin I to GND	0, V_{CC}	V
T_{oper}	Operating Ambient Temperature	-20, +70	°C
T_{stg}	Storage Temperature	-20, +150	°C

6407-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction Ambient Thermal Resistance	85	°C/W

6407-02.TBL

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, T_{amb} = 25°C, C_{load} = 20pF, R_{load} = 1kΩ, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
$V_{CC1,2}$	Supply Voltage		4.5	5	5.5	V
I_{CC1+2}	Supply Current		25	40	55	mA
R_R	Supply Voltage Rejection	f = 1kHz		40		dB
INPUTS						
V_{IN}	Signal Amplitude (all CVBS, Y, C inputs)		1.5	1.8		V_{PP}
V_{clamp}	Clamp Level (CVBS, Y inputs)		1.1	1.35	1.6	V
I_{clamp}	Clamp Current (CVBS, Y inputs)	V_{clamp} - 300mV		0.5	2	mA
I_{IN}	Leakage Current (CVBS, Y inputs)	V_{clamp} + 1V		0.5	2	µA
V_{DC}	Input DC Level (C, TRAP)		1.1	1.35	1.6	V
R_{IN}	Input Resistance (C inputs)		7	11	16	kΩ
R_{TRAP}	Input Resistance (TRAP input)		0. 75	1	1.25	kΩ
VIDEO OUTPUTS						
GV	Voltage Gain	V_{IN} = 1V_{PP} VOUT3 Other outputs	5.7 5.5	6.2 6	6.7 6.5	dB dB
B	Bandwidth (CVBS, Y/C adder)	C_{load} = 20pF att = -1dB att = -3dB		10 15		MHz MHz
CTK	Crosstalk Between Channels	f = 3.58MHz, V_{IN} = 1V_{PP} Same group input/output Diff. group input/output	 50 55	 55 60		 dB dB
R_{OUT}	Output Resistance			10	30	Ω
V_{sync}	Top Level Sync (Y or CVBS)		0.5	0.7	1	V
V_{bias}	Output Mean Level (chroma)		1.1	1.35	1.6	V
SOUT OUTPUT						
SO_L	SOUT Low Level	S1, S2, S3 < 0.8V			0.8	V
SO_M	SOUT Mid Level	1.3V < S1, S2, S3 < 3.5V	1.3	2.5	3.5	V
SO_H	SOUT High Level	S1, S2, S3 > 4.5V	4.5			V
R_{SOUT}	SOUT Output Impedance	(94C0), VOUT = 2.5V (94C4), VOUT = 0V (94CC), VOUT = 0V	0.1 1 0.1	0.5 3 0.8	1 5 1.6	kΩ kΩ kΩ
R_{SOUTI}	SOUT Output Impedance	(94C8), VOUT = 5V	1	5		MΩ

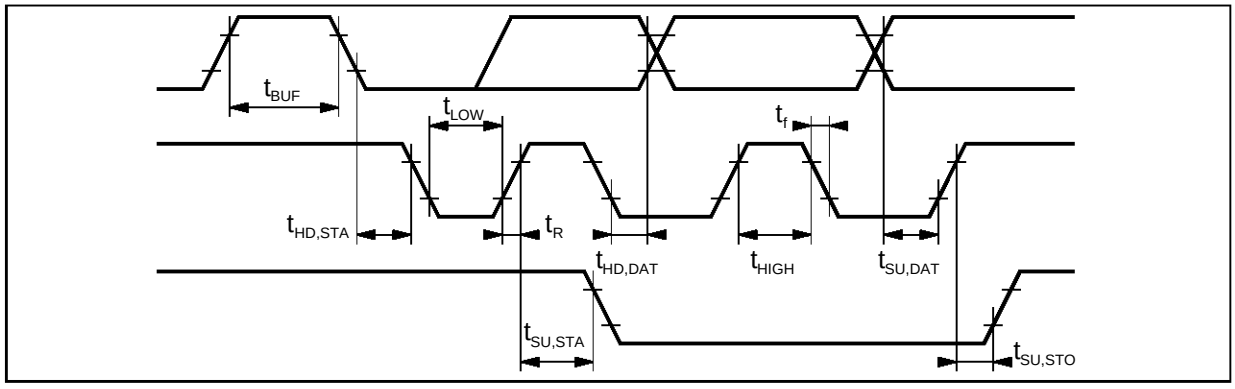
6407-03.TBL

I²C BUS CHARACTERISTICS

Symbol	Parameter	Test Conditions	Stand. Mode		Fast Mode		Unit
			Min.	Max.	Min.	Max.	
SCL							
V_{IL}	Low Level Input Voltage		-0.3	1.5	-0,3	1,5	V
V_{IH}	High Level Input Voltage		3	V_{CC}+0.5	3	V_{CC}+0.5	V
I_{LI}	Input Leakage Current	V_{IN} = 0 to V_{CC}	-10	10	-10	10	µA
f_{SCL}	Clock Frequency		0	100	0	400	kHz
t_R	Input Rise Time	1.5V to 3V		1,000		300	ns
t_F	Input Fall Time	1.5V to 3V		300		300	ns
C_I	Input Capacitance			10		10	pF
SDA							
V_{IL}	Low Level Input Voltage		-0.3	1.5	-0,3	1,5	V
V_{IH}	High Level Input Voltage		3	V_{CC}+0.5	3	V_{CC}+0.5	V
I_{LI}	Input Leakage Current	V_{IN} = 0 to V_{CC}	-10	10	-10	10	µA
C_I	Input Capacitance			10		10	pF
t_R	Input Rise Time	1.5V to 3V		1,000		300	ns
t_F	Input Fall Time	1.5V to 3V		300		300	ns
V_{OL}	Low Level Output Voltage	I_{OL} = 3mA		0.4		0.4	V
t_F	Output Fall Time	3V to 1.5V		250		250	ns
C_L	Load Capacitance			400		400	pF
TIMING							
t_{LOW}	Clock Low Period		4.7		1.3		µs
t_{HIGH}	Clock High Period		4		0.6		µs
$t_{SU,DAT}$	Data Set-up Time		250		100		ns
$t_{HD,DAT}$	Data Hold Time		0	340	0	340	ns
$t_{SU,STO}$	Set-up Time from Clock High to Stop		4		0.6		µs
t_{BUF}	Start Set-up Time Following a Stop		4.7		1.3		µs
$t_{HD,STA}$	Start Hold Time		4		0.6		µs
$t_{SU,STA}$	Start Set-up Time Following Clock Low to High Transition		4.7		0.6		µs

6407-04.TBL

Figure 1 : I²C Bus Timing



6407-03.EPS

I²C BUS SELECTION

Data transfers follow the usual I²C format : after the start condition (S), a 7-bit slave address is sent, followed by an eighth bit which is a data direction bit (R/W). Several successive data bytes can be sent in WRITE mode (R/W = 0) but only one status byte can be read at a time (R/W = 1).

String Format

S : Start condition - P : Stop condition - A : Acknowledge

Write Mode

S	SLAVE ADDRESS	0	A	DATA1	A	DATAN	A	P

Read Mode

S	SLAVE ADDRESS	1	A	STATUS	A	P

Slave Address

Address	A7	A6	A5	A4	A3	A2	A1	A0
Value	1	0	0	1	0	1	A1	R/W

A1 value depends on voltage on ADD input (V_{INADD}) :
- A1 = 0 if V_{INADD} < 0.4V (typ. : GND). Address : 94H
- A1 = 1 if V_{INADD} > 3.7V (typ. : V_{CC}). Address : 96H

Control Register (DATA1) (Write Mode)

		b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Output Group Selection	Output Group 1	0	0	X	X	X	X	X	X
	Output Group 2	0	1	X	X	X	X	X	X
	Output Group 3	1	0	X	X	X	X	X	X
Input Group Selection	V1	X	X	X	0	0	1	X	X
	V2	X	X	X	0	1	0	X	X
	V3	X	X	X	0	1	1	X	X
	Mute	X	X	1	1	0	0	0	0
	TV	X	X	1	1	0	0	1	0
	BS	X	X	1	1	0	1	1	0
	PIP	X	X	1	1	1	0	1	0
	MN-Y/MN-C	X	X	1	1	0	1	1	1
Input Format	Composite	X	X	X	X	X	X	1	0
	Y/C	X	X	X	X	X	X	1	1
SOUT Mode Selection	SOUT Not Modified	X	X	1	X	X	X	X	X
	SOUT Connected to S Input	X	X	0	X	X	X	X	X
SOUT Level Selection (Soft Mode)	SOUT < 0.8V	1	1	0	0	0	0	0	0
	1.3V < SOUT < 3.5V	1	1	0	0	0	1	0	0
	SOUT > 4.5V	1	1	0	0	1	1	0	0
	High Impedance (> 1MΩ)	1	1	0	0	1	0	0	0

Status Register (Read Mode)

b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
S3/b1	S3/b0	S2/b1	S2/b0	S1/b1	S1/b0	ID1-2	ID1-1

SX/bx : SX/b1 SX/b0 Voltage on S Inputs

	0	0	V_{IN} < 0.8V
	0	1	1.3V < V_{IN} < 3.5V
	1	1	V_{IN} > 4.5V

ID1-X : Voltage on ID1 Inputs

0	< 0.4V
1	> 3.7V

I²C BUS SELECTION

Power-on Reset

Power-on reset is active when the power supply voltage is over 4V. Then, the device is in the following configuration :

- All outputs except YOUT2 and COUT2 are muted.
- SOUT is in high impedance state.

PIN CONFIGURATIONS

Figure 2 : Y & CVBS Inputs (Pins 2-6-9-10-12 and Pins 14-15-28-34-40-41-44)

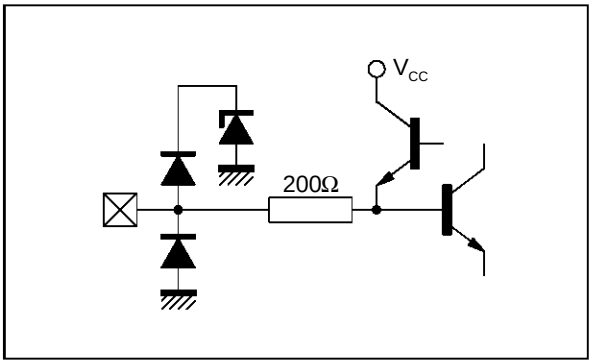


Figure 3 : C Inputs (Pins 4-8-16-26-32-42)

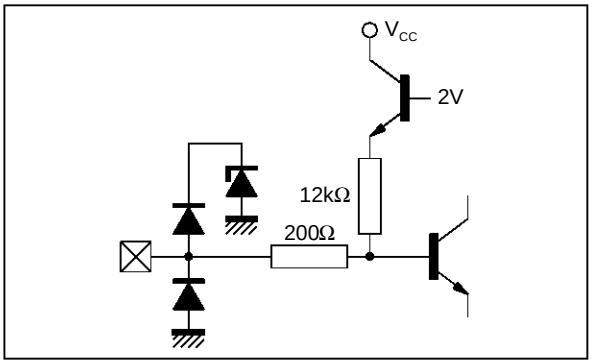


Figure 4 : ID1-1, ID1-2 Inputs, Add (Pins 3-5-27)

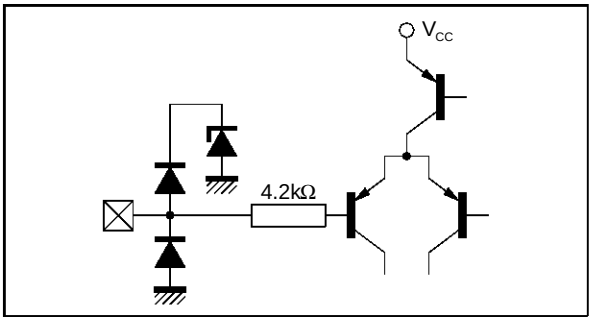


Figure 5 : 6dB Amplifier Outputs (Pins 24-25-29-30-31-35-36)

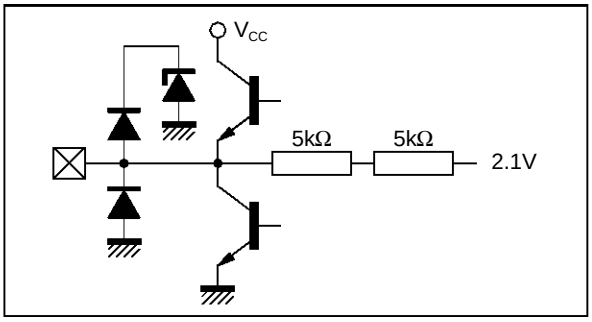


Figure 6 : Trap Filter Input (Pin 38)

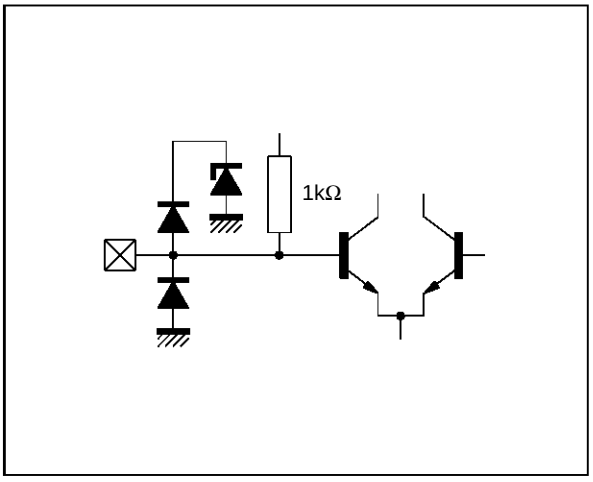
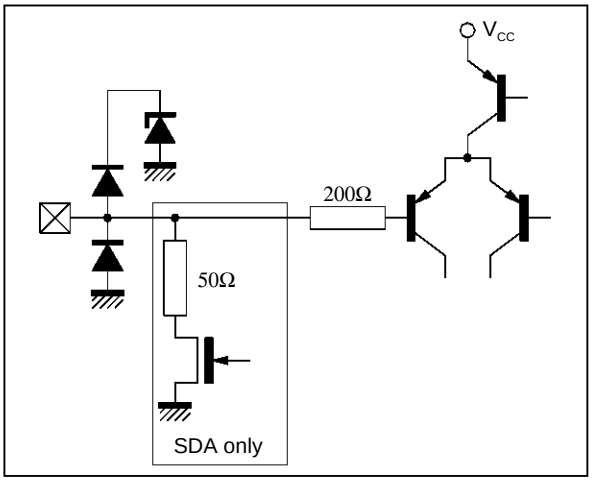


Figure 7 : I²C Bus Pins SDA, SCL (Pins 20-21)



PIN CONFIGURATIONS (continued)

Figure 8 : OUT Output (Pin 33)

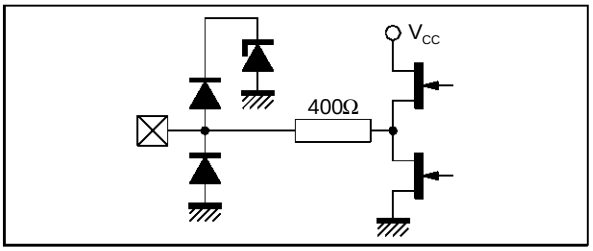


Figure 9 : Power Supplies (Pins 18-19)
(V_{CC1} : Analog , V_{CC2} : Logic)

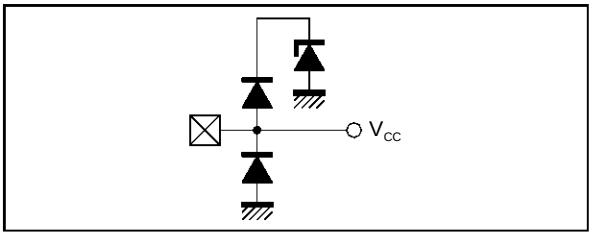
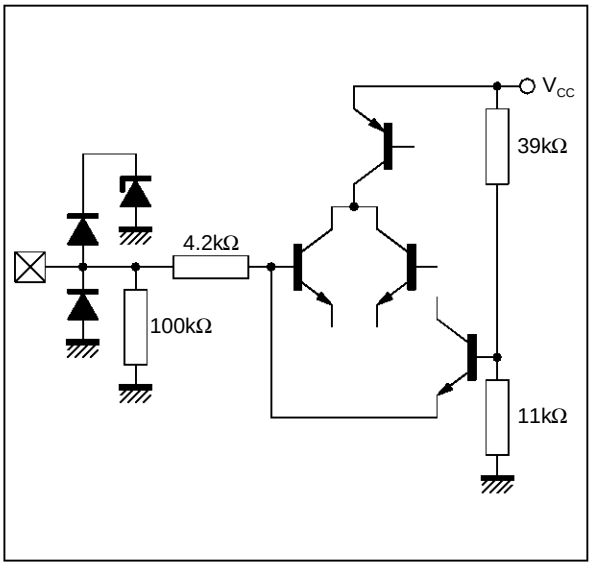
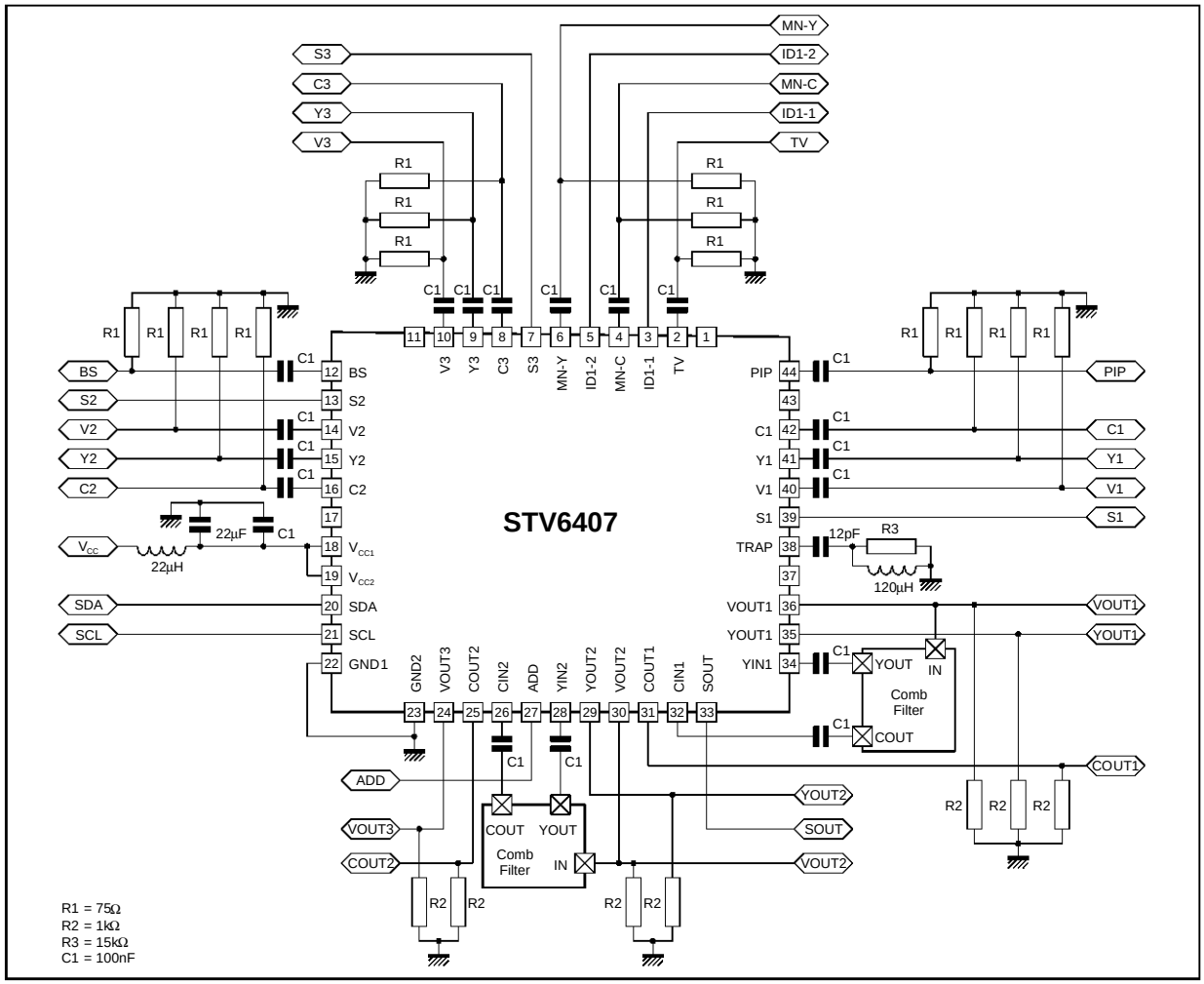


Figure 10 : S1, S2, S3 Inputs (Pins 7-13-39)

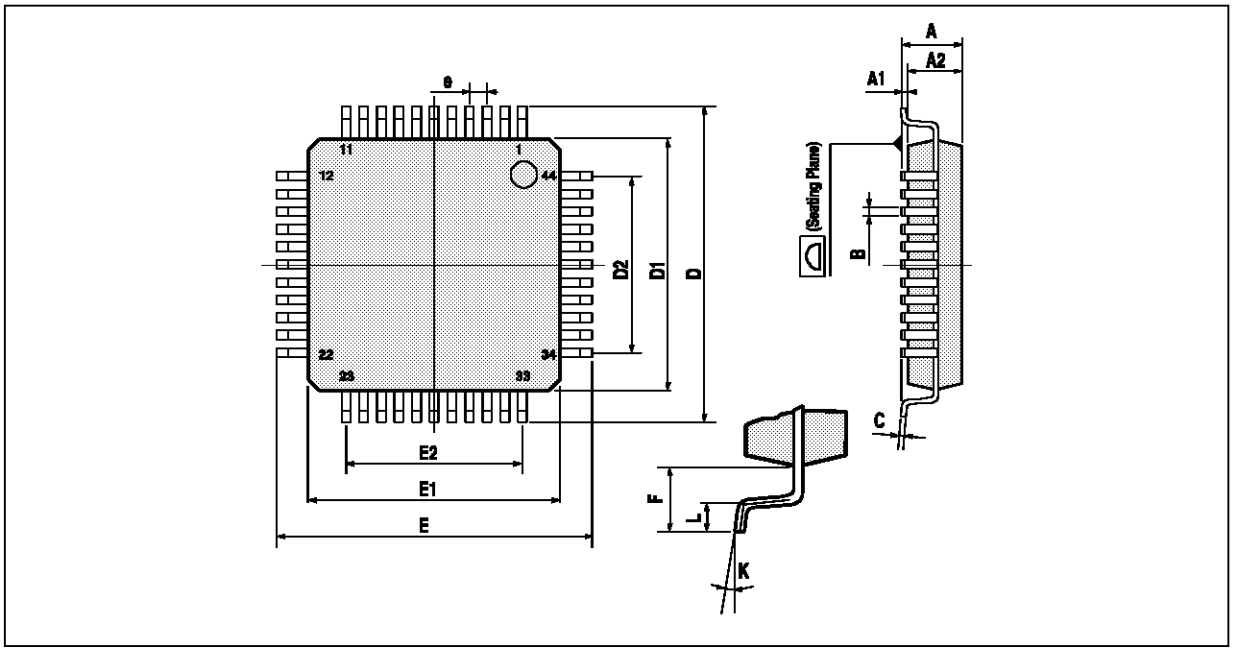


TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

44 PINS - PLASTIC QUAD FLAT PACK



PMPQFP44.WMF

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.45			0.096
A1	0.25			0.01		
A2	1.95	2.00	2.10	0.077	0.079	0.083
B	0.30		0.45	0.012		0.018
C	0.13		0.23	0.005		0.009
D	12.95	13.20	13.45	0.51	0.52	0.53
D1	9.90	10.00	10.10	0.390	0.394	0.398
D2		8.00			0.315	
e		0.80			0.031	
E	12.95	13.20	13.45	0.510	0.520	0.530
E1	9.90	10.00	10.10	0.390	0.394	0.398
E2		8.00			0.315	
F		1.60			0.063	
K	0^o (min.), 7^o (max.)					
L	0.65	0.80	0.95	0.026	0.031	0.037

PQFP44.TBL

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